B.Sc. Semester-III Examination, 2022-23

ELECTRONICS [Honours]

Course ID : 31712 Course Code : SH/ELC/302/C-6(T)

Course Title : Digital Electronics and Verilog

Time : 1 Hour 15 Minutes. Full Marks : 25

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

1. Answer any **three** of the following questions: 1×3=3

   a) How many half adders and full adders will be required to add two 26-bit numbers?

   b) What is combinational circuit? Give one example.

   c) What is the difference between a decoder and a de-multiplexer (DMUX)?

   d) Mention the name of the logic gate which is used as equality detector.

   e) Draw the logic circuit of a one-bit comparator.

   f) What is a half adder? Give its truth table.

2. Answer any **three** of the following questions: 2×3=6

   a) Perform the relation:

      i) $(AF.59)_{16} = (?)_8$

      ii) $(45)_{10} - (95)_{10}$

      using 2's complement method.

   b) i) Add 4318 and 7678 in 8421 BCD (Binary Coded Decimal),

      ii) Perform $(—15)_{10} + (—26)_{10}$ using l's complement method.

   c) In MOS logic, CMOS is preferred over P-MOS and N-MOS. Why?

   d) What is Tri-state logic? What type of arrangement is necessary for that?

   e) What is a parallel adder? Construct an n-bit parallel adder with full adder and half adder.

   f) What is flip-flop? How many stable states are there in a flip-flop?

3. Answer any **two** of the following questions: 5×2=10

   a) Explain the working of a half-subtractor with logic diagram and truth table. Realize it using NAND gate only. 5

b) Draw the logic diagram of a 3-bit ripple counter. Draw the output wave form of the counter and explain its operations. 2+3=5

c) Draw the logic symbol of clocked R-S flip-flop and give its truth table. How will you get D and T flip-flops from J-K flipflops? 3+2=5

d) Minimize the following expression using K-map and realize using NOR gates only–

$f(P, Q, R, S) = \Pi(1, 4, 6, 9, 10, 11, 14, 15)$.

4. Answer any **one** of the following questions: 6×1=6

a) Design a 3-bit shift resistor using J-K flip-flops. Write down different modes of operations of the shift resistor. 4+2=6

b) Construct a TTL NAND gate. Explain its principle of operation. What is totem-pole arrangement of a circuit? How this circuit can be modified into tri-state inverter? 2+2+2=6

c) Give the internal organization of a 16×4 memory chip. What is memory expansion? How is it done? Give the logic symbol of a 256×4 ROM. 2+1+1+2=6

————————